

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)} max	Package	I _D max T _A = +25°C
Q1	30V	55mΩ @ V _{GS} = 10V	TSOT26	3.8A
		65mΩ @ V _{GS} = 4.5V	TSOT26	3.6A
Q2	-30V	110mΩ @ V _{GS} = -10V	TSOT26	-2.5A
		142mΩ @ V _{GS} = -4.5V	TSOT26	-2.1A

Features

- Complementary MOSFET
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description

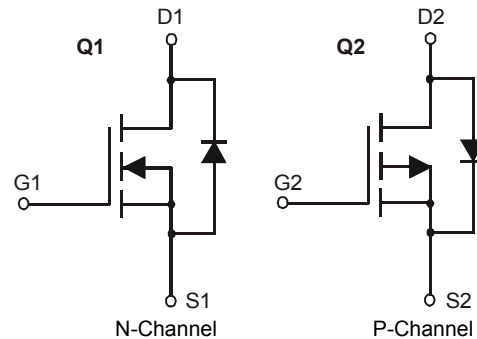
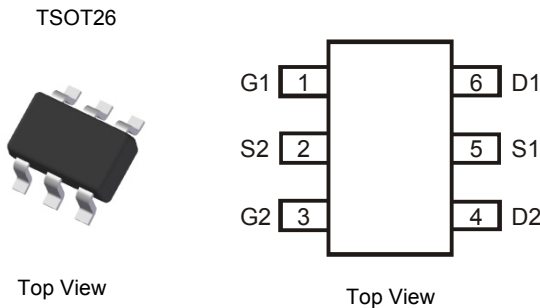
This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.008 grams (approximate)



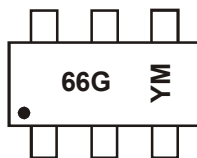
Device Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMG6601LVT-7	TSOT26	3K/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



66G = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: X = 2010)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings - Q1 and Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Q1	Q2	Units	
Drain-Source Voltage	V _{DSS}	30	-30	V	
Gate-Source Voltage	V _{GSS}	±12	±12	V	
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	3.8 3.0	-2.5 -2	A
	t < 10s	T _A = +25°C T _A = +70°C	4.5 3.4	-3 -2.3	A
Maximum Body Diode Forward Current (Note 6)	I _S	1.5	-1.5	A	
Pulsed Drain Current (Note 6)	I _{DM}	20	-15	A	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P _D	T _A = +25°C	0.85
		T _A = +70°C	0.54
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	Steady state	147
		t < 10s	103
Total Power Dissipation (Note 6)	P _D	T _A = +25°C	1.3
		T _A = +70°C	0.83
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	Steady state	96
		t < 10s	67
Thermal Resistance, Junction to Case (Note 6)	R _{θJC}	36	
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics - Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current @T _J = +25°C	I _{DSS}	-	-	1	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	±100	nA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	0.5	1	1.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	-	34	55	mΩ	V _{GS} = 10V, I _D = 3.4A
		-	38	65		V _{GS} = 4.5V, I _D = 3A
		-	49	85		V _{GS} = 2.5V, I _D = 2A
Forward Transfer Admittance	Y _{fs}	-	6	-	S	V _{DS} = 5V, I _D = 3.4A
Diode Forward Voltage (Note 7)	V _{SD}	-	0.75	1.0	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	-	422	-	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	-	41	-	pF	
Reverse Transfer Capacitance	C _{rss}	-	39	-	pF	
Gate resistance	R _g	-	1.26	-	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	-	5.4	-	nC	V _{GS} = 10V, V _{DS} = 15V, I _D = 3.1A
Total Gate Charge (V _{GS} = 10V)	Q _g	-	12.3	-	nC	
Gate-Source Charge	Q _{gs}	-	0.8	-	nC	
Gate-Drain Charge	Q _{gd}	-	1.2	-	nC	
Turn-On Delay Time	t _{D(on)}	-	1.6	-	ns	V _{DS} = 15V, V _{GS} = 10V, R _L = 4.7Ω, R _G = 3Ω,
Turn-On Rise Time	t _r	-	7.4	-	ns	
Turn-Off Delay Time	t _{D(off)}	-	31.2	-	ns	
Turn-Off Fall Time	t _f	-	15.6	-	ns	

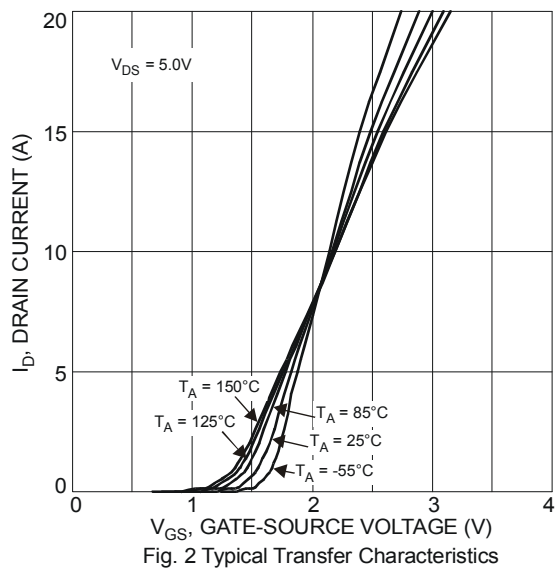
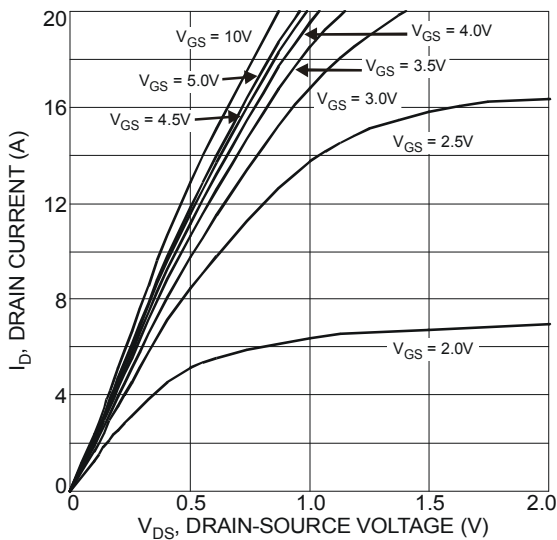
- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1 inch square copper plate
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

Electrical Characteristics - Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	-	-	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current @T _J = +25°C	I _{DSS}	-	-	-1	μA	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	±100	nA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.4	-0.8	-1.2	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(on)}	-	70	110	mΩ	V _{GS} = -10V, I _D = -2.3A
		-	81	142		V _{GS} = -4.5V, I _D = -2A
		-	105	190		V _{GS} = -2.5V, I _D = -1A
		-	-	-		V _{GS} = -2.5V, I _D = -1A
Forward Transfer Admittance	Y _{fs}	-	5.3	-	S	V _{DS} = -5V, I _D = -2.3A
Diode Forward Voltage (Note 7)	V _{SD}	-	-0.8	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	-	541	-	pF	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	-	46	-	pF	
Reverse Transfer Capacitance	C _{rss}	-	43	-	pF	
Gate resistance	R _g	-	16.9	-	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	-	6.5	-	nC	V _{GS} = -10V, V _{DS} = -15V, I _D = -2.3A
Total Gate Charge (V _{GS} = -10V)	Q _g	-	13.8	-	nC	
Gate-Source Charge	Q _{gs}	-	1.0	-	nC	
Gate-Drain Charge	Q _{gd}	-	1.6	-	nC	
Turn-On Delay Time	t _{D(on)}	-	1.7	-	ns	V _{DS} = -15V, V _{GS} = -10V, R _L = 6Ω, R _G = 3Ω,
Turn-On Rise Time	t _r	-	4.6	-	ns	
Turn-Off Delay Time	t _{D(off)}	-	18.3	-	ns	
Turn-Off Fall Time	t _f	-	2.2	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

N Channel - Q1



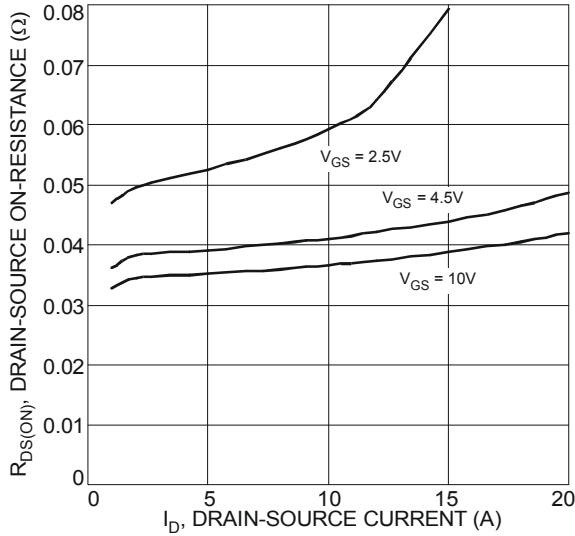


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

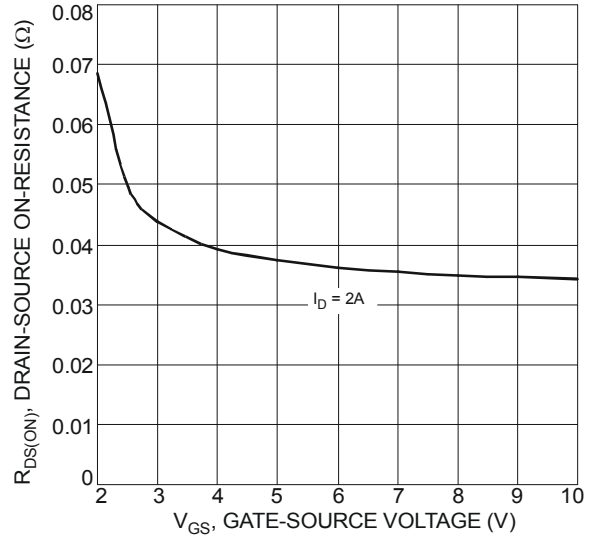


Fig. 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

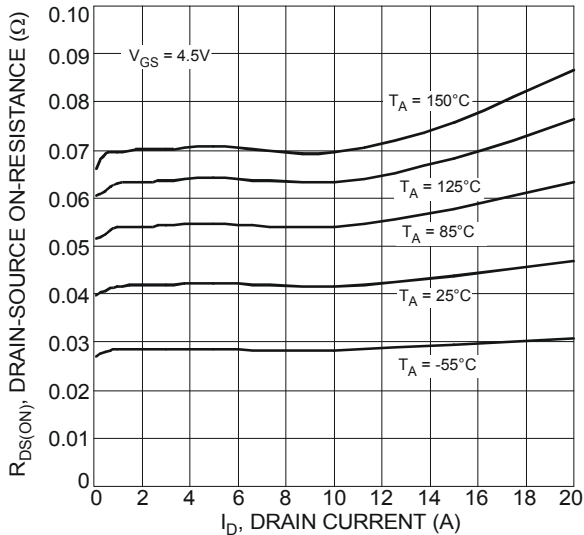


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

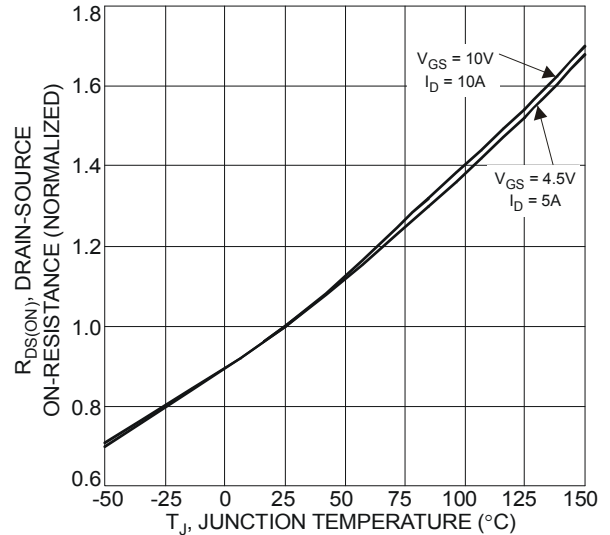


Fig. 6 On-Resistance Variation with Temperature

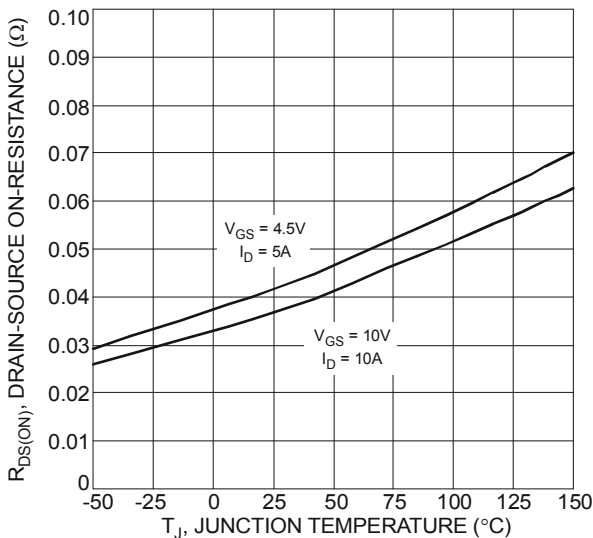


Fig. 7 On-Resistance Variation with Temperature

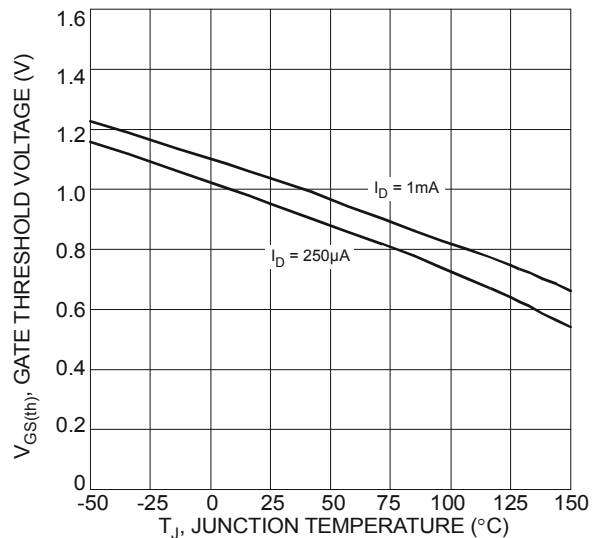


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

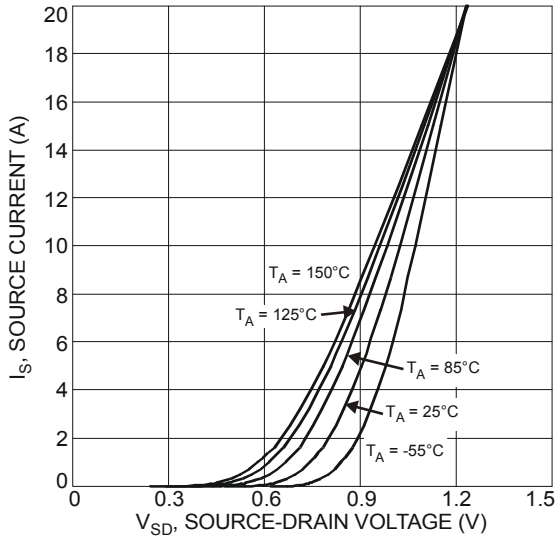


Fig. 9 Diode Forward Voltage vs. Current

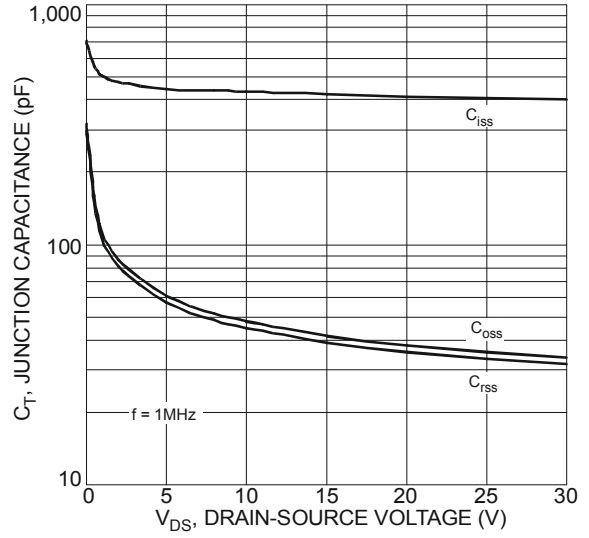


Fig. 10 Typical Junction Capacitance

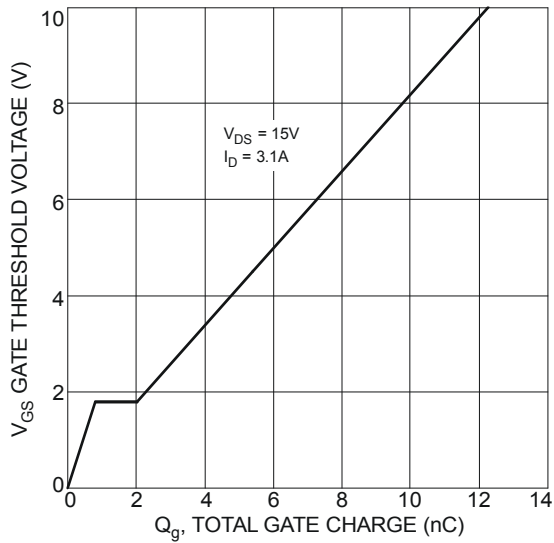


Fig. 11 Gate Charge

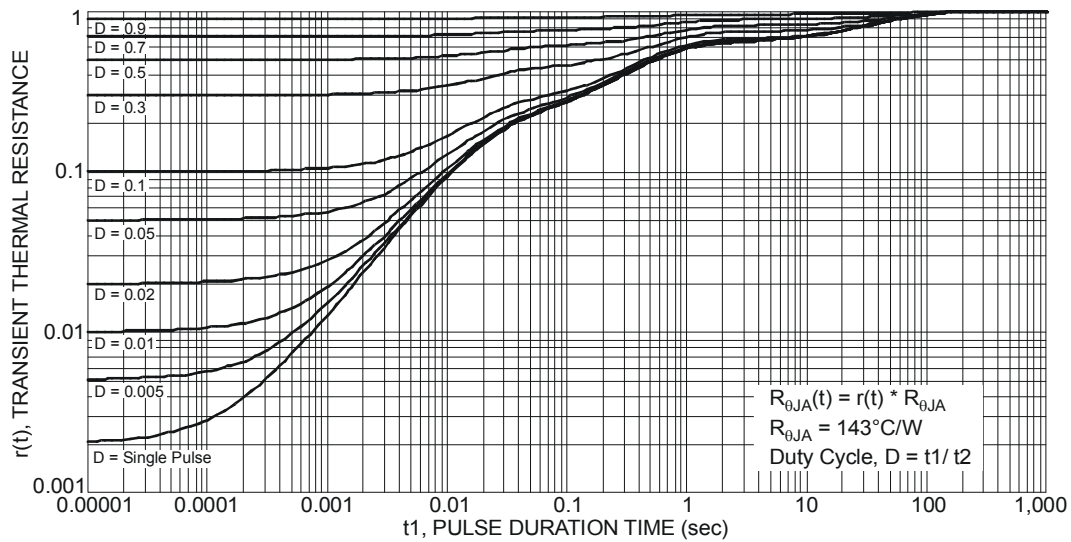


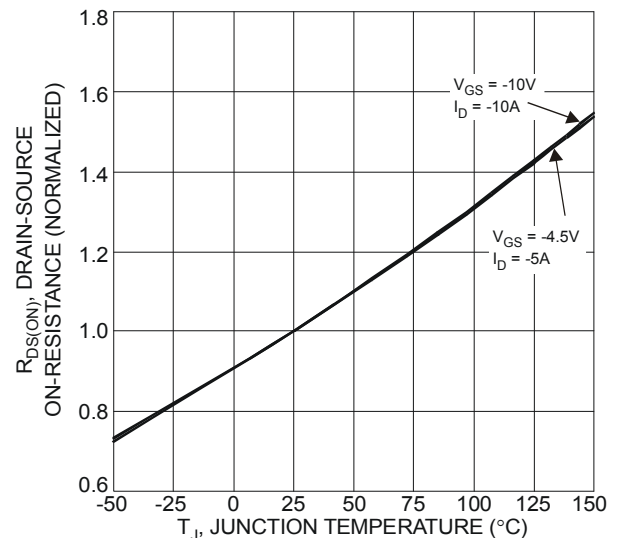
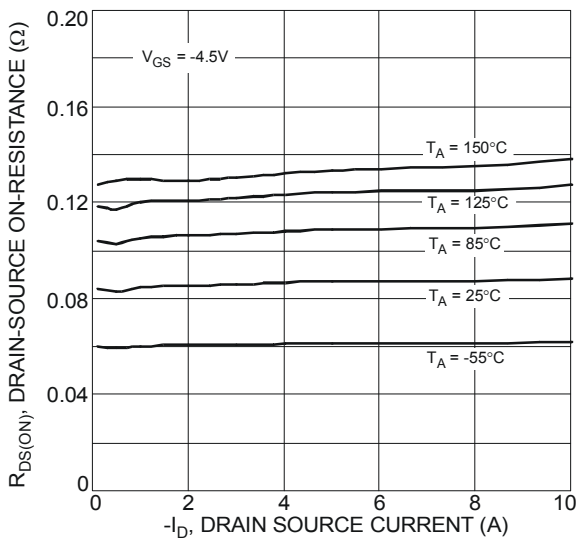
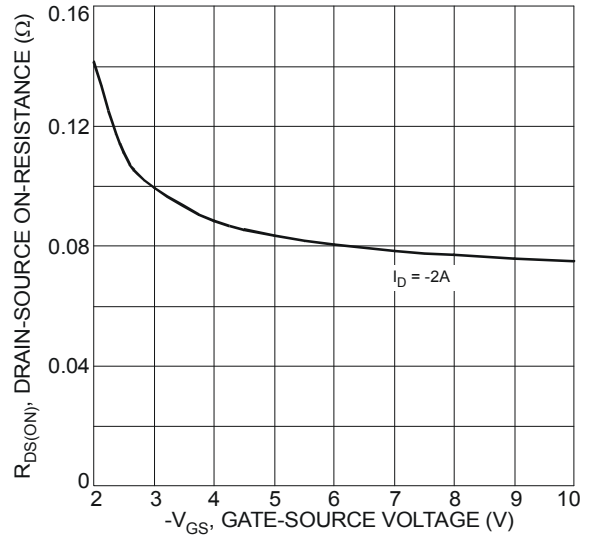
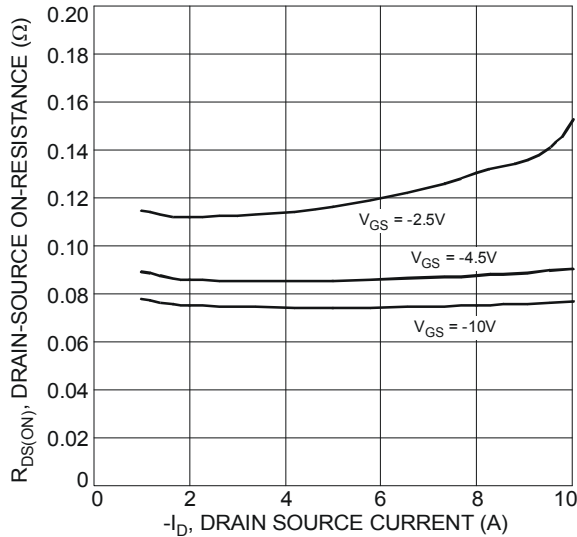
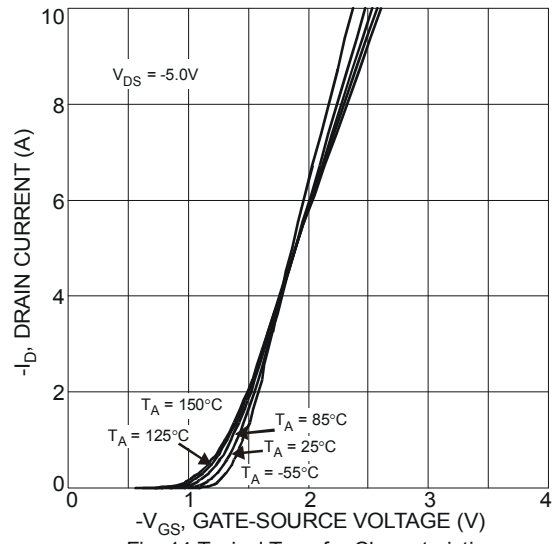
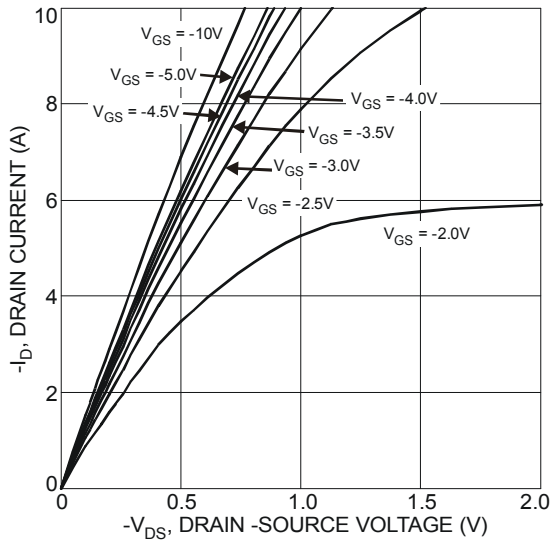
Fig. 12 Transient Thermal Resistance

$$R_{\theta JA}(t) = r(t) * R_{\theta JA}$$

$$R_{\theta JA} = 143^{\circ}\text{C/W}$$

$$\text{Duty Cycle, } D = t_1 / t_2$$

P Channel - Q2



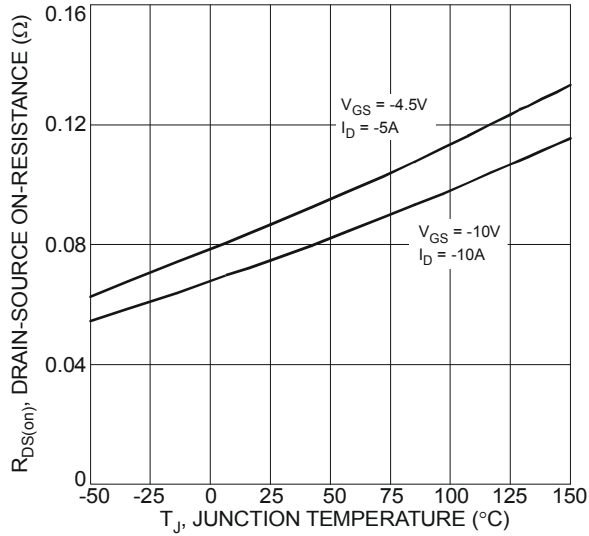


Fig. 19 On-Resistance Variation with Temperature

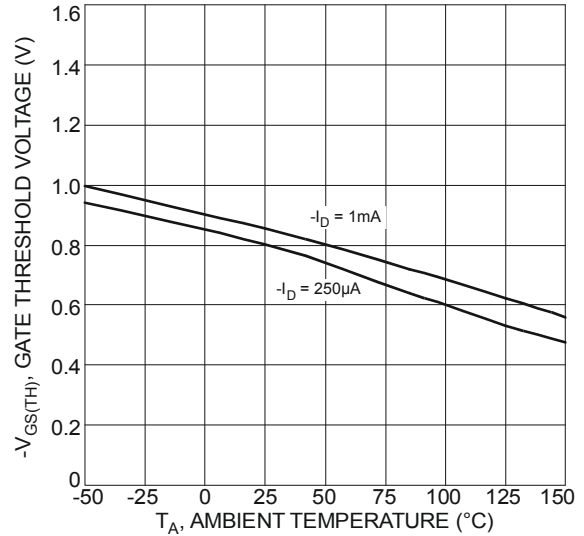


Fig. 20 Gate Threshold Variation vs. Ambient Temperature

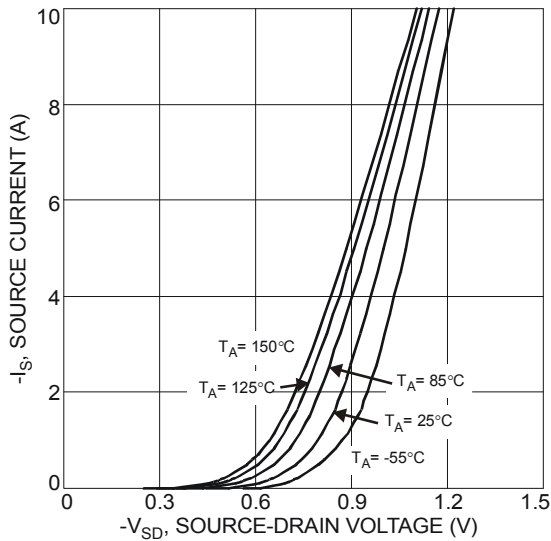


Fig. 21 Diode Forward Voltage vs. Current

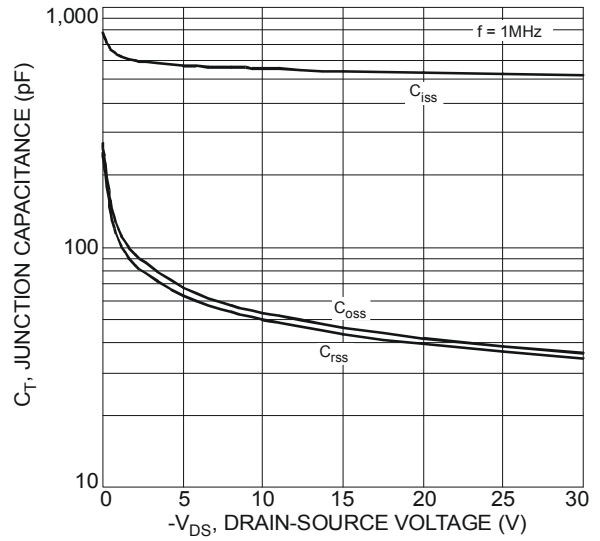


Fig. 22 Typical Junction Capacitance

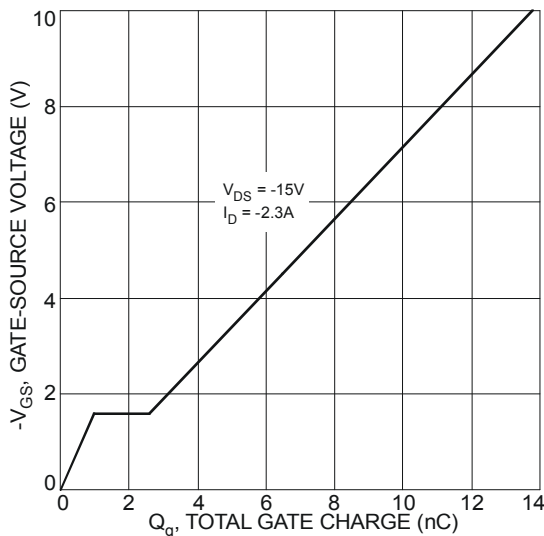
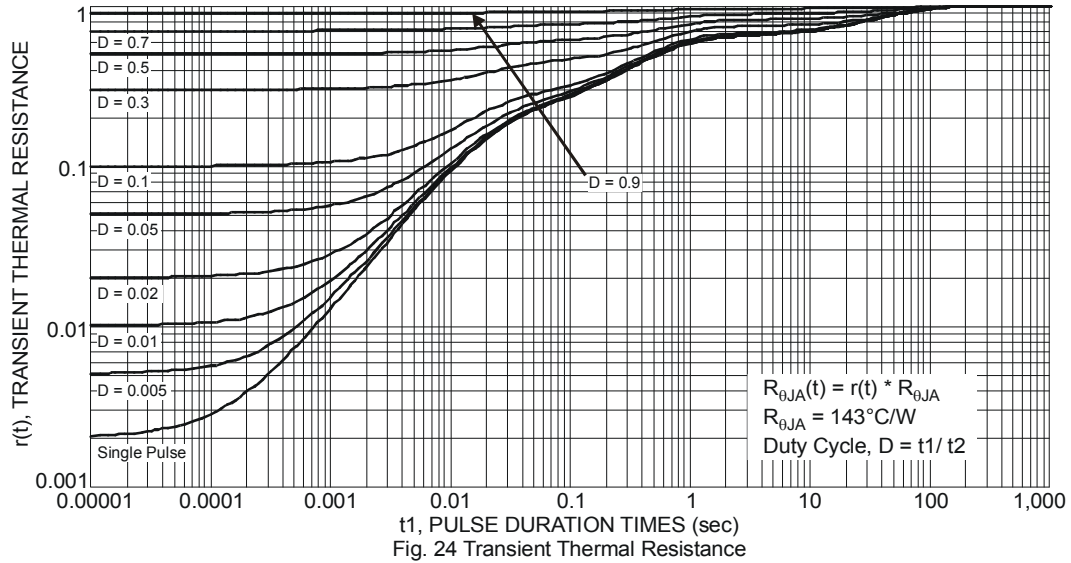
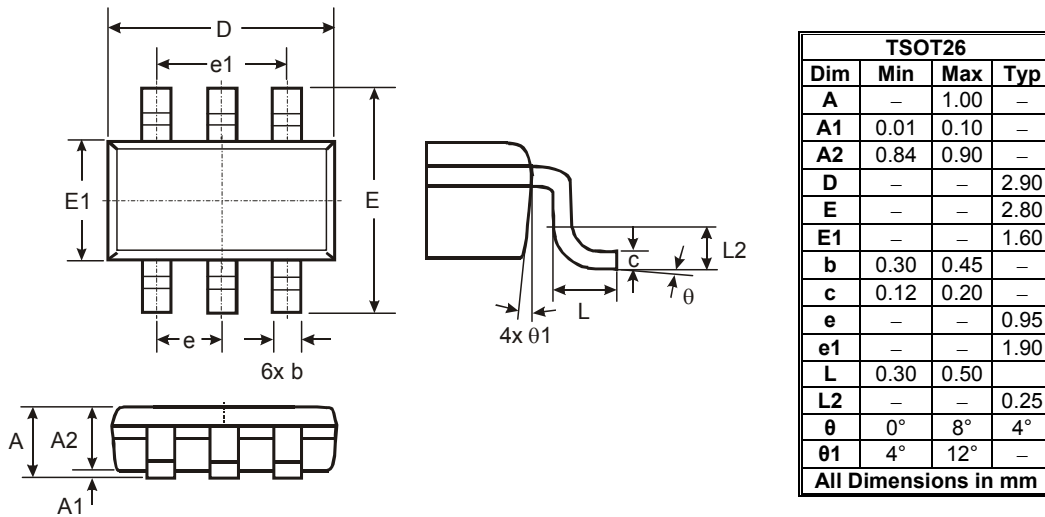


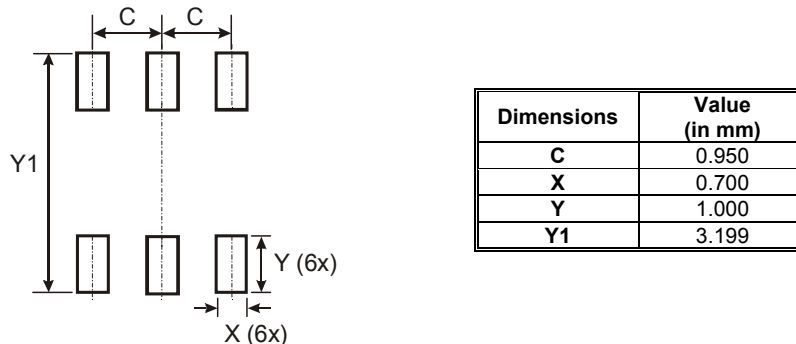
Fig. 23 Gate-Charge Characteristics



Package Outline Dimensions



Suggested Pad Layout



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